CLAIMS

What is claimed is:

1. A method for synchronizing a plurality of processors of a multi-processor computer system on a synchronization point, comprising:

triggering a first set of processors, using a lead processor of said plurality of processors when said lead processor encounters said synchronization point, to enter an exit holding loop, said first set of processors representing said plurality of processors except said lead processor, said triggering said first set of processors being performed without accessing a shared memory area of said multi-processor system; and

triggering said plurality of processors, using a tail processor of said plurality of processors when said tail processor encounters said synchronization point, to leave said exit holding loop, said triggering said plurality of processors being performed without accessing said shared memory area of said multi-processor system.

2. The method of claim 1 further comprising

creating a circular reference arrangement for said plurality of processors, one of said plurality of processors being designated said lead processor, another one of said processors being designated said tail processor, said lead processor being adjacent to said tail processor in said circular reference arrangement.

3. The method of claim 2 wherein said circular reference arrangement represents a circular linked list.

4. The method of claim 2 wherein said triggering said first set of processors is performed in a cascading manner starting with said lead processor following a sequence established by said circular reference arrangement, with each processor of said first set of processors being triggered by its immediate predecessor in said sequence.

5. The method of claim 4 wherein said triggering said plurality of processors is performed in a cascading manner starting with said tail processor following said sequence established by said circular reference arrangement, with each processor of said plurality of processors being triggered by its immediate predecessor in said sequence.

6. The method of claim 5 further comprising

enabling processors of said first set of processors to enter an entry holding loop if said processors of said first set of processors encounter said instruction before said lead processor.

7. The method of claim 6 wherein said triggering said first set of processors employs a first external interrupt mechanism associated with each of said first set of processors.

8. The method of claim 7 wherein said triggering said first set of processors includes writing to hard physical addresses of each of said first set of processors.

9. The method of claim 6 wherein said triggering said plurality of processors employs a second external interrupt mechanism associated with each of said plurality of processors.

10. The method of claim 9 wherein said triggering said plurality of processors includes writing to hard physical addresses of each of said plurality of processors.

11. The method of claim 1 wherein said triggering said first set of processor employs a masked interrupt approach.

12. An article of manufacture comprising a program storage medium having computer readable code embodied therein, said computer readable code being configured to synchronize a plurality of processors of a multi-processor computer system on a synchronization point, comprising:

computer readable code for triggering a first set of processors, using a lead processor of said plurality of processors when said lead processor encounters said synchronization point, to enter an exit holding loop, said first set of processors representing said plurality of processors except said lead processor, said triggering said first set of processors being performed without accessing a shared memory area of said multi-processor system; and

computer readable code for triggering said plurality of processors, using a tail processor of said plurality of processors when said tail processor encounters said synchronization point, to leave said exit holding loop, said triggering said plurality of processors being performed without accessing said shared memory area of said multi-processor system.

13. The article of manufacture of claim 12 further comprising

computer readable code for creating a circular reference arrangement for said plurality of processors, one of said plurality of processors being designated said lead processor, another one of said processors being designated said tail processor, said lead processor being adjacent to said tail processor in said circular reference arrangement.

14. The article of manufacture of claim 13 wherein said circular reference arrangement represents a circular linked list.

15. The article of manufacture of claim 13 wherein said triggering said first set of processors is performed in a cascading manner starting with said lead processor following a sequence established by said circular reference arrangement, with each processor of said first set of processors being triggered by its immediate predecessor in said sequence.

16. The article of manufacture of claim 15 wherein said triggering said plurality of processors is performed in a cascading manner starting with said tail processor following said sequence established by said circular reference arrangement, with each processor of said plurality of processors being triggered by its immediate predecessor in said sequence.

17. The article of manufacture of claim 16 further comprising

computer readable code for enabling processors of said first set of processors to enter an entry holding loop if said processors of said first set of processors encounter said instruction before said lead processor.

18. The article of manufacture of claim 17 wherein said triggering said first set of processors employs a first external interrupt mechanism associated with each of said first set of processors.

19. The article of manufacture of claim 18 wherein said computer readable code for triggering said first set of processors includes computer readable code for writing to hard physical addresses of each of said first set of processors.

20. The article of manufacture of claim 17 wherein said triggering said plurality of processors employs a second external interrupt mechanism associated with each of said plurality of processors.

21. The article of manufacture of claim 20 wherein said computer readable code for triggering said plurality of processors includes computer readable code for writing to hard physical addresses of each of said plurality of processors.

22. The article of manufacture of claim 12 wherein said computer readable code for triggering said plurality of processors include computer readable code for receiving trigger signals using a masked interrupt approach.

23. A method for synchronizing a plurality of processors of a multi-processor computer system on a synchronization point in instantiations of a computer program, comprising:

implementing a circular reference arrangement for said plurality of processors, each of said plurality of processors having an immediately preceding processor and an immediately succeeding processor, one of said plurality of processors being designated said lead processor, another one of said processors being designated said tail processor, said lead processor immediately succeeding said tail processor in said circular reference arrangement;

keeping a first set of processors in an entry holding loop when said processors of said first set of processors reach said synchronization point, said first set of processors representing said plurality of processors except said lead processor;

cascade triggering along said circular reference arrangement said first set of processors, using a lead processor of said plurality of processors when said lead processor encounters said synchronization point, to enter an exit holding loop, said cascade triggering said first set of processors being performed without accessing a shared memory area of said multi-processor system;

keeping said lead processor in said exit holding loop; and thereafter

cascade triggering along said circular reference arrangement said plurality of processors, using a tail processor of said plurality of processors when said tail processor encounters said synchronization point, to leave said exit holding loop, said cascade triggering said plurality of processors being performed without accessing said shared memory area of said multi-processor system.

24. The method of claim 23 wherein said circular reference arrangement represents a circular linked list.

25. The method of claim 23 wherein said cascade triggering said first set of processors employs a first external interrupt mechanism associated with each of said first set of processors.

26. The method of claim 25 wherein said cascade triggering said first set of processors includes writing to hard physical addresses of each of said first set of processors.

27. The method of claim 25 wherein said cascade triggering said plurality of processors employs a second external interrupt mechanism associated with each of said plurality of processors.

28. The method of claim 27 wherein said cascade triggering said plurality of processors includes writing to hard physical addresses of each of said plurality of processors.

29. The method of claim 23 wherein said cascade triggering employs a masked interrupt approach.